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(58) Field of search
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INT CL^s H04N

(54) Television standard conversion apparatus

(57) A television standards conversion apparatus having less picture quality degradation caused by flicker or distortion for converting a signal from the 625/50 standard to the 525/60 standard includes a digital field memory 2 for converting the field frequency followed by a scanning line interpolator 3 which converts the spatial positions of the scanning lines, and finally a digital line memory 4 for converting the number of scanning lines from 625 to 525. The memories are controlled by two clock generators 6, 7 having different clock frequencies.

In an alternative arrangement a digital field memory 10 converts the field frequency and the scanning line number and provides two similar outputs one line period displaced which are fed to a scanning line interpolator 11.

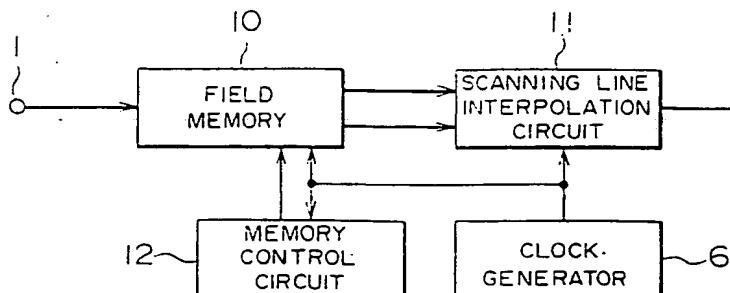
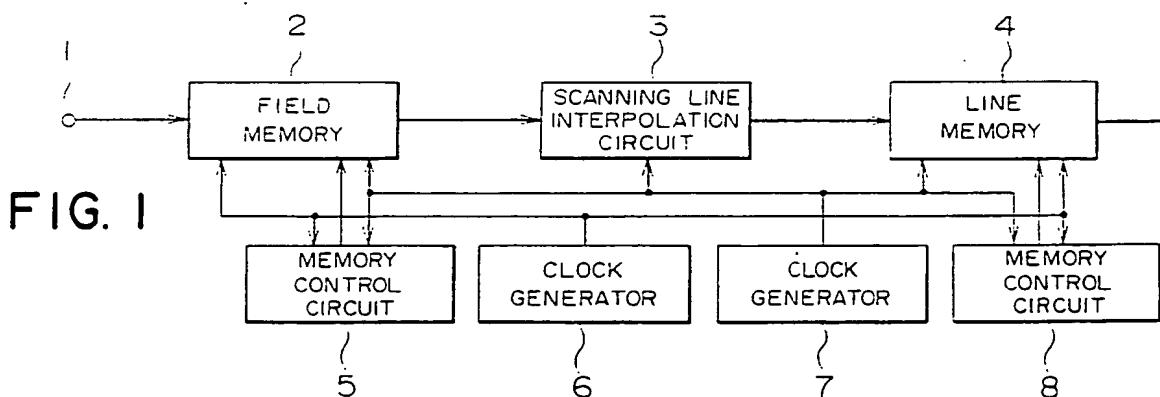


FIG. 1

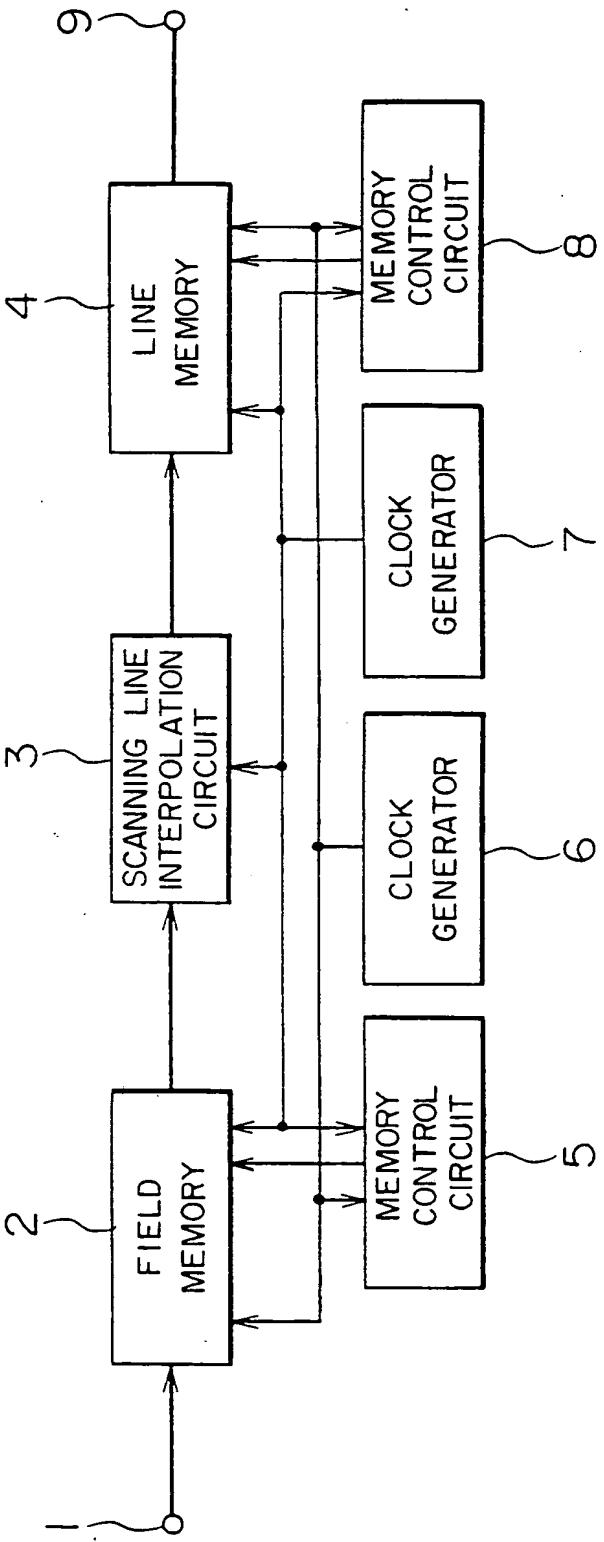


FIG. 2

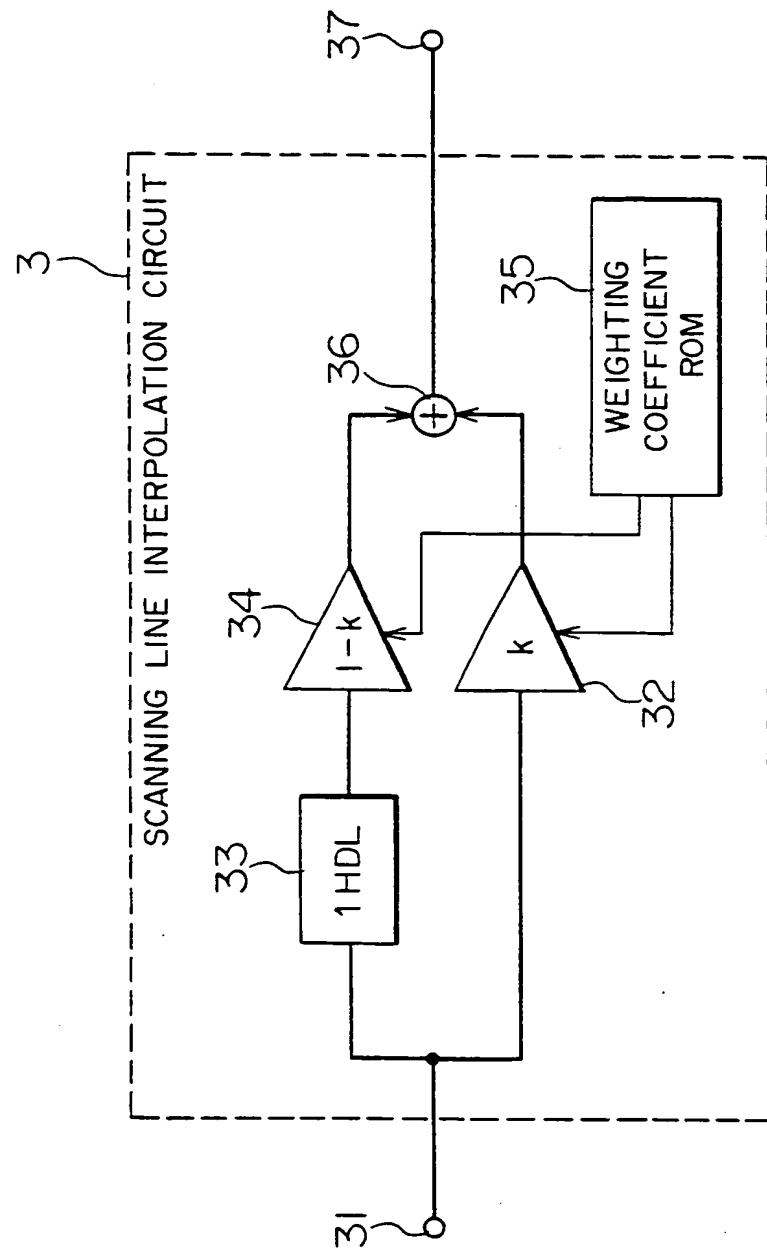


FIG. 3

FIELD MEMORY WRITING SIDE
FIELD FREQUENCY 50 Hz

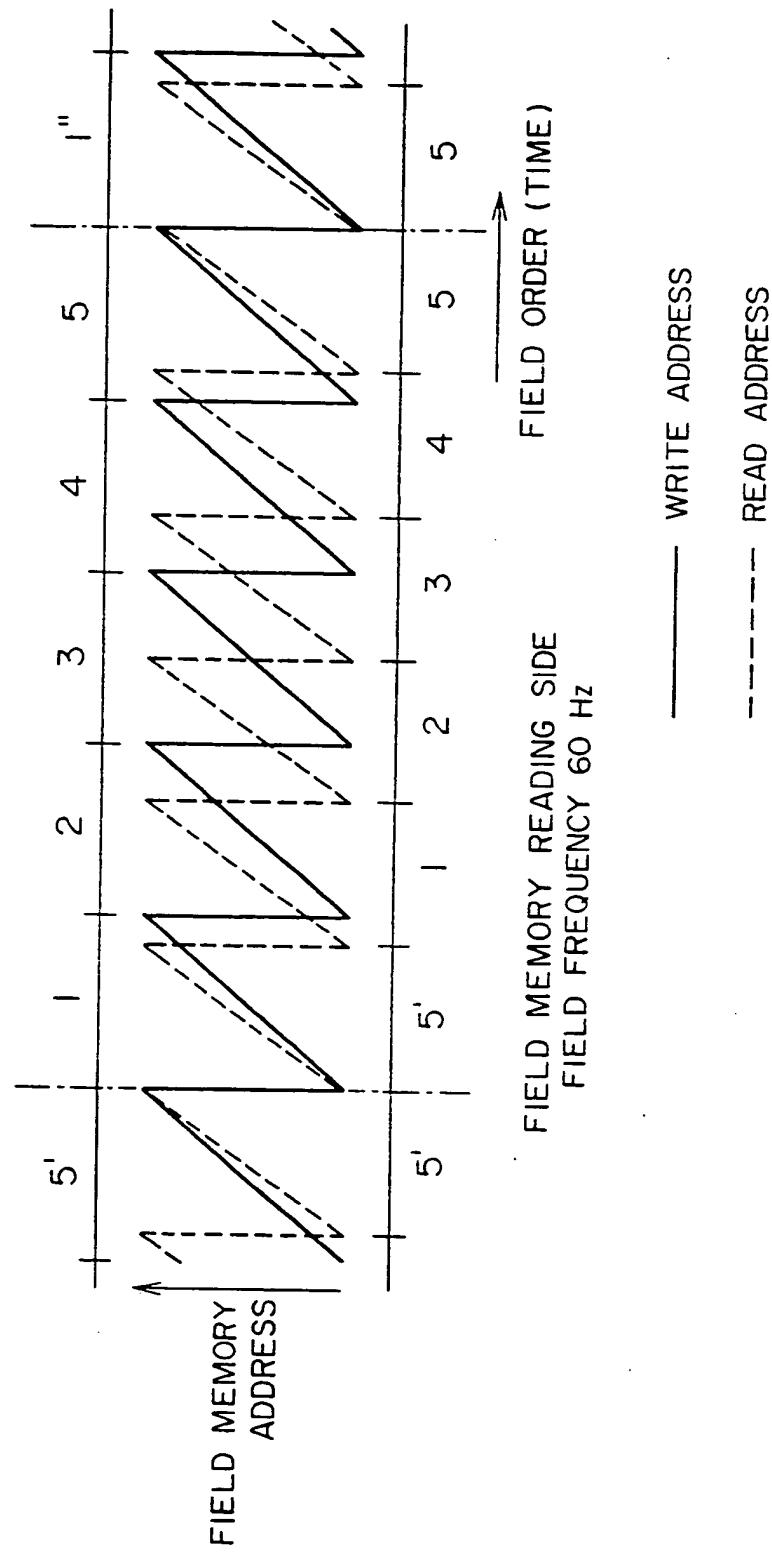


FIG. 4

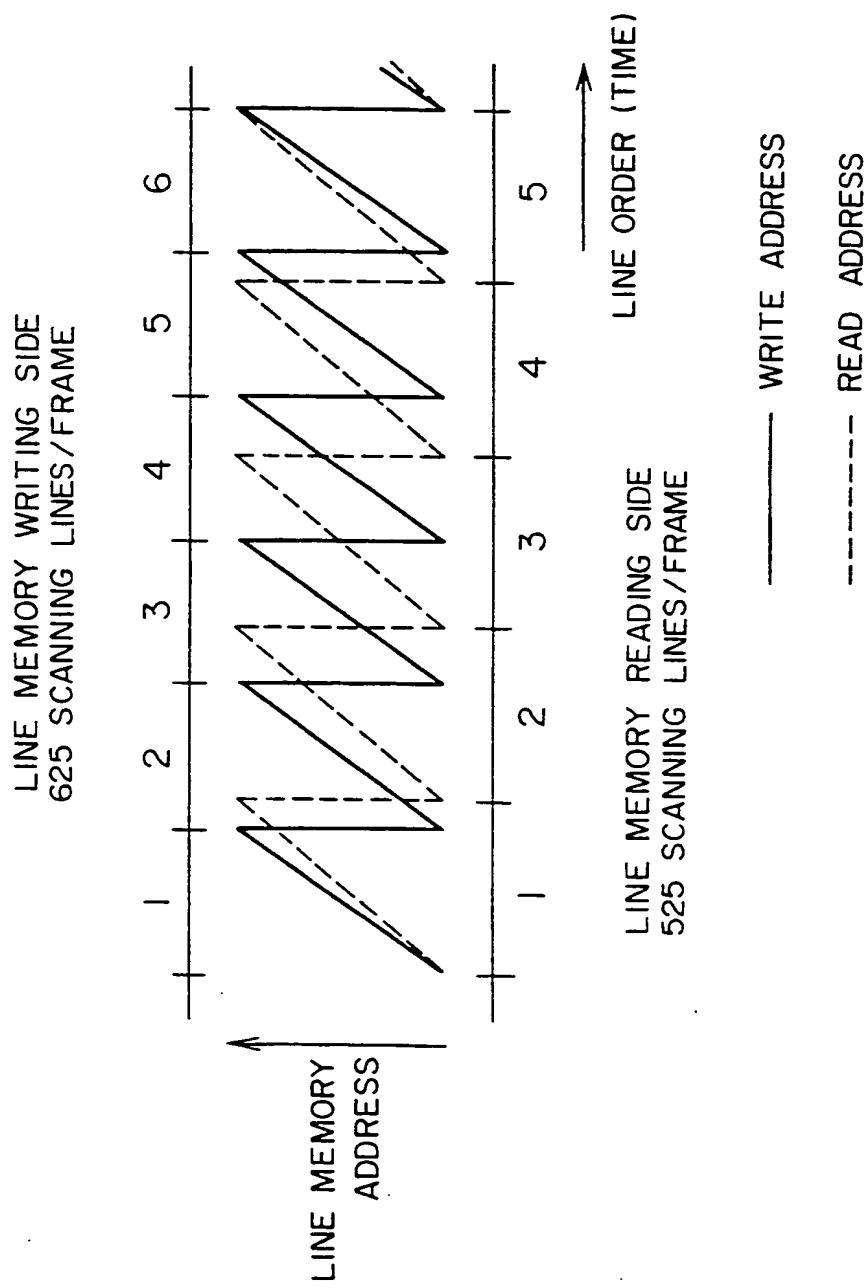


FIG. 5A

ODD FIELDS
OF 625/50 →
STANDARD

ODD FIELDS
OF 525/60 →
STANDARD

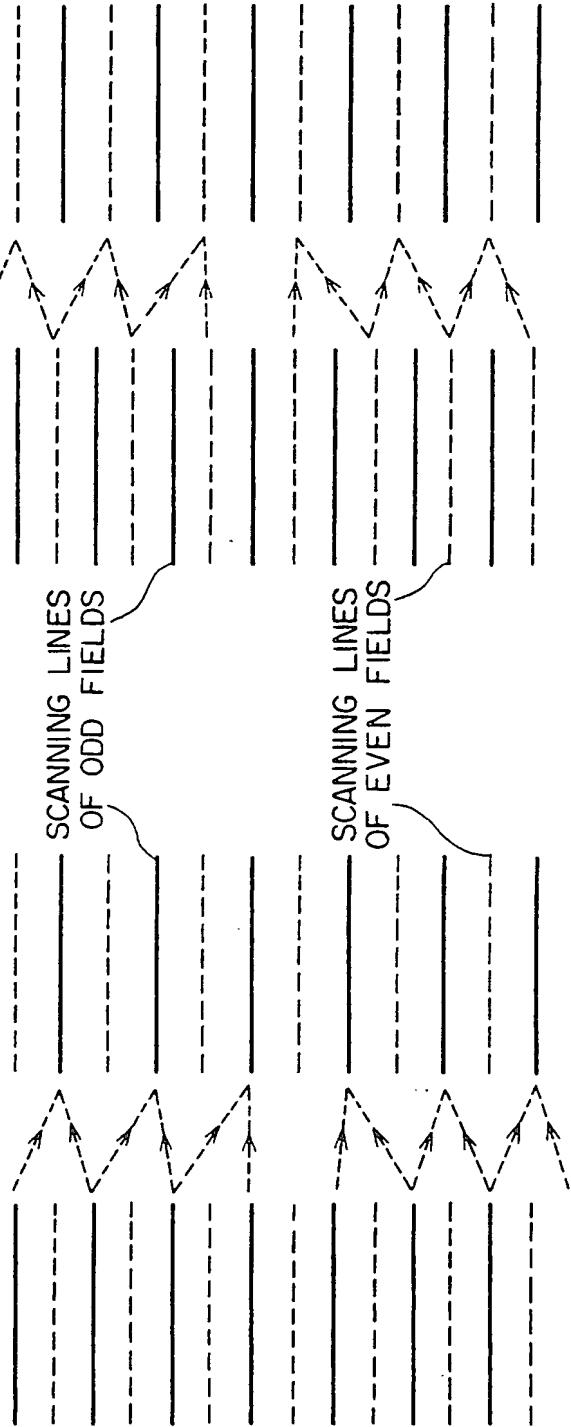


FIG. 5B

EVEN FIELDS
OF 625/50 →
STANDARD

EVEN FIELDS
OF 525/60 →
STANDARD

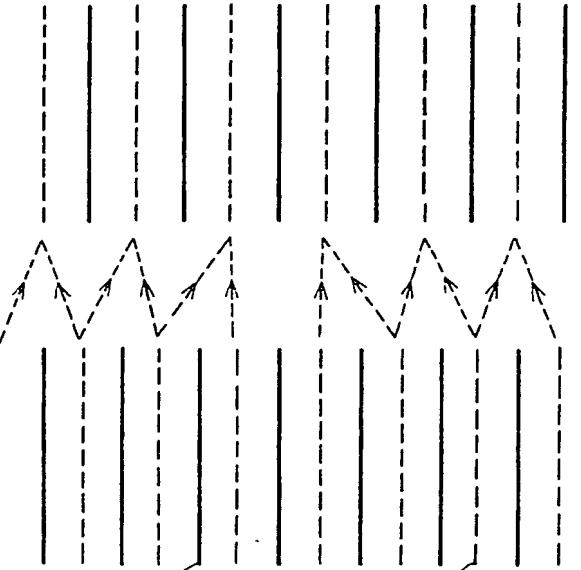


FIG. 5C

ODD FIELDS
OF 625/50 →
STANDARD

EVEN FIELDS
OF 625/50 →
STANDARD

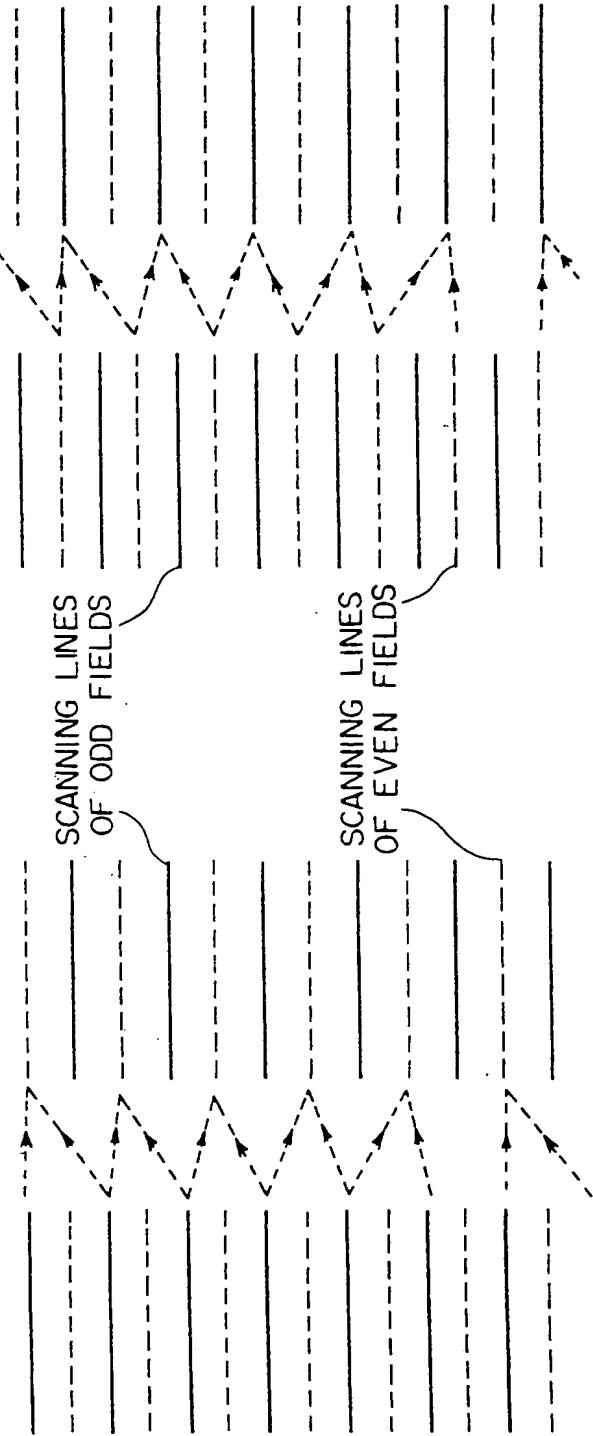


FIG. 5D

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7/10

FIG. 6

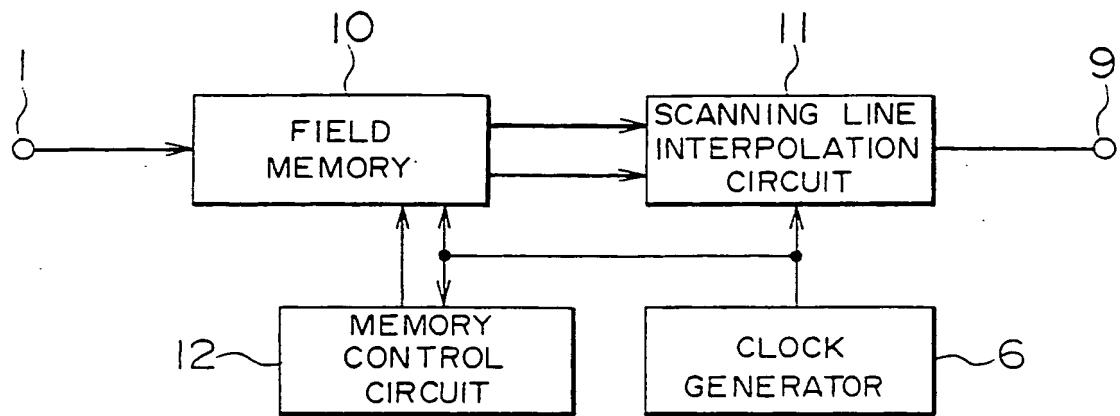


FIG. 7

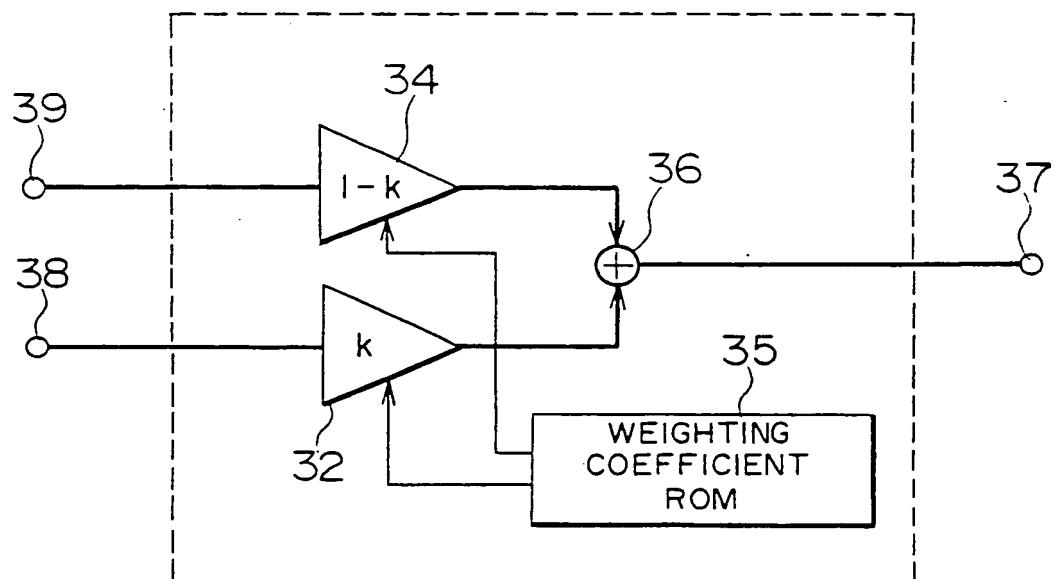
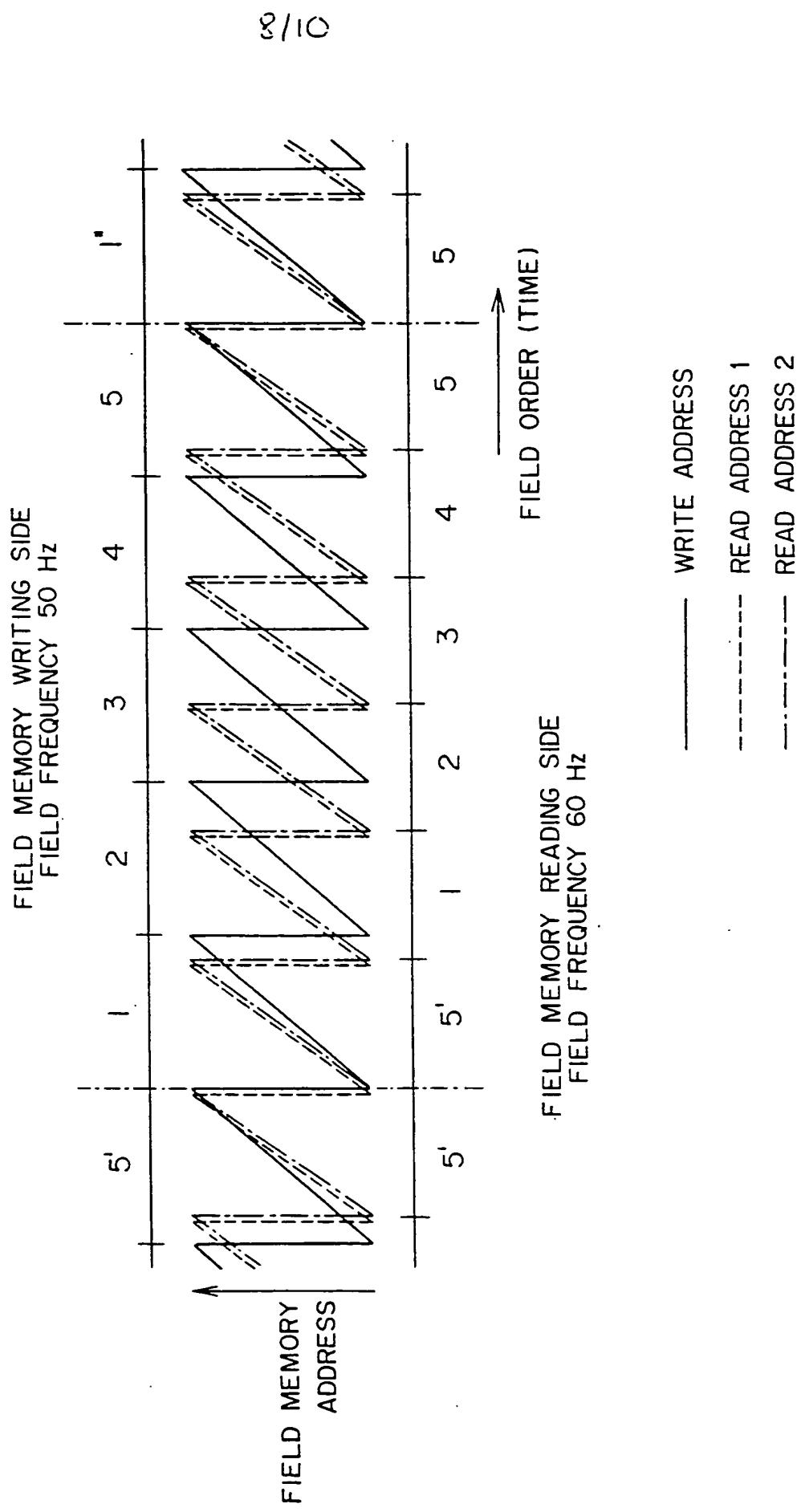


FIG. 8



3/10

FIG. 9

625/50 STANDARD -----> 525/60 STANDARD

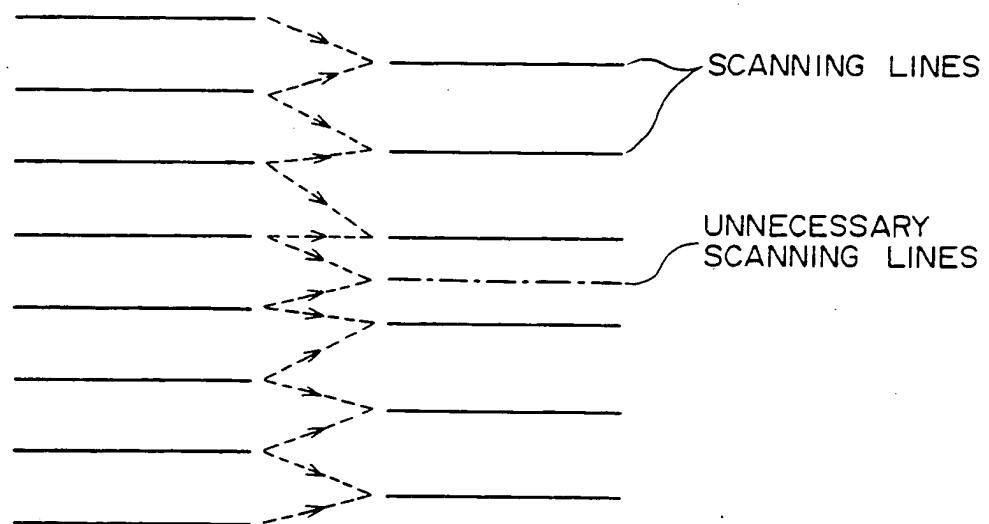
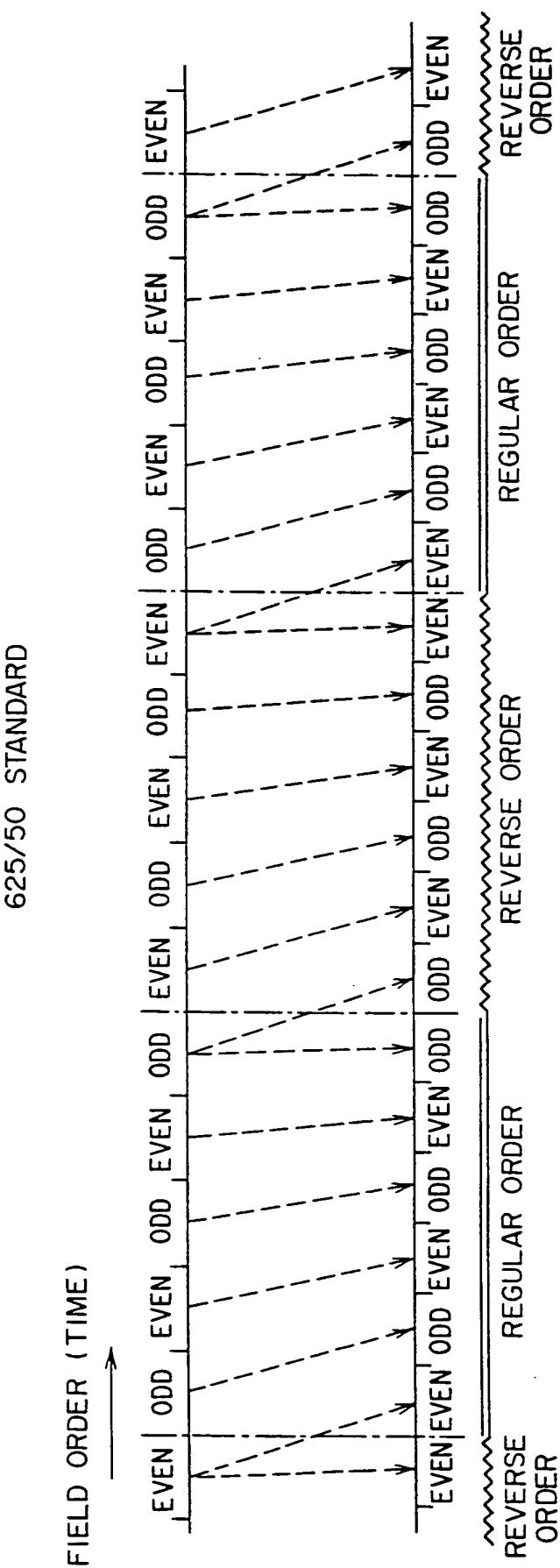


FIG. I

10/10.



TELEVISION STANDARD CONVERSION APPARATUS

1 BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a television standards conversion apparatus for converting the number 5 of scanning lines and the field frequency of video signals into those of another television standards.

DESCRIPTION OF THE RELATED ART

Conversion in television standards from a video signal of the 625/50 standard having the number of 10 scanning lines equivalent to 625 and a field frequency of 50 Hz to a video signal of the 525/60 standard having the number of scanning lines equivalent to 525 and a field frequency of 60 Hz is achieved by conversion in the number of scanning lines and field frequency. Such 15 conversion in the number of scanning lines and field frequency is typically performed by digital signal processing using digital memories and so on as described in ITEJ Technical Report Vol. 14, No. 32, pp. 1-6 (June 1990).

20 Its configuration and operation will hereafter be described with reference to Figs. 9 and 10 for the case where a television signal inputted to be converted is a PAL component signal of the 625/50 standard and it is to be converted into an NTSC component signal of 25 525/60 standard and outputted. Fig. 9 is a schematic

1 diagram showing an example of conventional scanning line
interpolation processing. Fig. 10 is a diagram for
explaining how conventional field frequency conversion
is performed by means of repetition of a signal of field
5 unit.

A digitized component signal of PAL standard
is inputted from an input terminal. From the PAL signal
having 625 scanning lines per frame, an NTSC signal
having 525 scanning lines per frame is produced in a
10 scanning line interpolation circuit by scanning line
interpolation processing for converting spatial
positions of scanning lines as shown in Fig. 9. In Fig.
9, positions of respective scanning lines correspond to
spatial positions on the screen. By the scanning line
15 interpolation processing, two PAL scanning lines are
weighted and combined to interpolate NTSC scanning lines
as shown in Fig. 9. In the conventional example,
however, a signal which is not necessary as the NTSC
signal as represented by a phantom line is also inter-
20 polated in the ratio of approximately six to one. In
fact, 525 scanning lines, which are required as the NTSC
signal and which are represented by solid lines in Fig.
9, and 100 scanning lines which are not required as the
NTSC signal, i.e., a total of 625 scanning lines per
25 frame are outputted from the scanning line interpolation
circuit to a field memory. On the basis of a control
signal fed from a memory control circuit, it is
inhibited to write scanning lines, which are included in

1 625 inputted scanning lines per frame and which are not
 required as the NTSC signal, into the field memory,
 whereas only 525 scanning lines which are required as
 the NTSC signal are written into the field memory. That
5 is to say, scanning line decimation is performed on 625
 scanning lines to produce 525 scanning lines. At the
 time of writing scanning lines into the memory, scanning
 lines are decimated from 625 to 525 per frame, i.e., at
 a rate of 5/6. In reading scanning lines from the field
10 memory, therefore, the signal can be read out repeti-
 tively by taking a field as the unit at the rate of one
 field every five fields as shown in Fig. 10. By reading
 out repetitively the signal corresponding to one field
 with respect to five-field input, six fields are out-
15 putted. Thus the field frequency is converted from 50
 Hz of the PAL standard to 60 Hz of the NTSC standard. A
 component signal, which has been converted from the PAL
 standard to the NTSC standard by the operation hereto-
 fore described, is outputted from an output terminal.

20 In such a conventional scanning line number
 and field frequency conversion circuit in the television
 standards conversion apparatus, scanning line inter-
 polation is performed and thereafter repetition of the
 field unit for field frequency conversion is performed.
25 Therefore, the state in which odd fields and even fields
 are correctly outputted alternately is not brought about
 as shown in Fig. 10. Thus the field sequence relation
 is not maintained.

1 In case an odd field and an even field are
 outputted in a reverse order in the conventional
 example, therefore, the odd field and the even field are
 respectively outputted as an even field and an odd field
5 by replacing a vertical synchronizing signal. When this
 method is used, the state in which odd fields and even
 fields are normally outputted and the state in which an
 odd field is outputted as an even field and an even
 field is outputted as an odd field are repeated every
10 six fields. In the image reproduced from the converted
 signal of the 525/60 standard, therefore, a flicker of
 10 Hz swinging finely upward and downward is caused,
 resulting in picture quality degradation.

For preventing such a flicker, it is
15 considered to conduct processing of interpolating
 scanning lines on the readout side of the field memory.
 By reading out one field repetitively from the field
 memory every five fields, the field frequency is
 converted from 50 Hz to 60 Hz. This signal thus
20 converted in field frequency is subject to scanning line
 interpolation processing for converting spatial posi-
 tions from scanning lines of 625/50 standard to scanning
 lines of 525/60 standard. At this time, field attribute
 alteration is performed. That is to say, if the field
25 sequence relation of the output signal holds true,
 scanning line interpolation processing from an odd field
 of 625/50 standard to an odd field of 525/60 standard or
 scanning line interpolation processing from an

1 even field of 625/50 standard to an even field of 525/60
standard is performed. If the field sequence relation
of the output signal is reversed, scanning line inter-
polation processing from an odd field of 625/50 standard
5 to an even field of 525/60 standard or scanning line
interpolation processing from an even field of 625/50
standard to an odd field of 525/60 standard is per-
formed. By doing so, the field sequence relation of the
output signal is always maintained and an interpolated
10 scanning line is outputted on the correct position on
the screen. Therefore, flickers swinging finely upward
and downward are not caused.

In case scanning line interpolation processing
is performed on the readout side of the field memory as
15 described above, however, the signal of one field is
repetitively read out from the field memory every five
fields to convert the field frequency from 50 Hz to 60
Hz. For thus reading the signal of one field repeti-
tively, the number of scanning lines per field must be
20 limited to 5/6. That is to say, readout must be per-
formed while decimating one scanning line every six
scanning lines. As a result, precision of scanning line
interpolation in the position corresponding to the scan-
ning line decimated on the converted screen is degraded.

25 SUMMARY OF THE INVENTION

In view of these points, an object of the
present invention is to provide a television standards

1 conversion apparatus having scanning line number and
field frequency conversion means which does not cause
picture quality degradation due to scanning line
decimation in conducting scanning line interpolation
5 processing on the readout side of the field memory.

In order to achieve this object, a television standards conversion apparatus of the present invention (Claim 1) includes clock generation means for generating a first clock and a second clock; time-axis compression 10 and field frequency conversion means for writing a digitized component signal of 625/50 television standards into a first digital memory with the first clock generated by the above described clock generation means, for performing time-axis compression on the signal when 15 reading out the signal stored in the above described first digital memory with the second clock generated by the above described clock generation means, for converting a field frequency of the 625/50 television standards to a field frequency of the 525/60 television standards 20 by reading out the signal repetitively by taking a field as the unit at the rate of one field every five fields, and for outputting the resultant signal as a signal corresponding to 625 scanning lines/60 Hz; scanning line interpolation means for performing scanning line interpolation processing for converting odd/even field attribute and converting spatial positions of scanning lines on the above described signal compressed on the time axis and converted in field frequency; and time- 25

1 axis expansion and scanning line number conversion means
for writing the above described signal having inter-
polated scanning lines into a second digital memory with
the second clock generated by the above described clock
5 generation means, for decimating scanning lines from 625
per frame to 525 per frame when reading out the signal
stored in the above described second digital memory with
the first clock generated by the above described clock
generation means, and for expanding the signal on the
10 time axis to restore the rate of the original clock and
output the resultant signal.

A television standards conversion apparatus of
the present invention (Claim 2) includes field frequency
and scanning line number conversion means for writing a
15 digitized component signal of 625/50 television stand-
ards into a digital memory having two output standards
allowing readout from mutually independent addresses,
converting the field frequency and the number of scan-
ning lines to the field frequency and the number of
20 scanning lines of the 525/60 television standards by
conducting scanning line decimation processing and
repetition of a signal while taking a field as the unit
when reading the signal from the above described digital
memory having two output standards, and for deriving the
25 resultant signal from a first output terminal; memory
control means for deriving, from a second output of the
above described digital memory, a signal which is 1H
away from the signal subjected to the conversion in

1 field frequency and the number of scanning lines and
derived from the first output of the above described
digital memory; and scanning line interpolation means
for performing scanning line interpolation processing
5 for converting odd/even field attribute and converting
spatial positions of scanning lines on the signal, which
has been converted in field frequency and the number of
scanning lines and derived from the above described
first output, by using the above described signal which
10 is 1H away derived from the second output, and for
thereby converting the above described signal, which has
been converted in field frequency and the number of
scanning lines, into a signal of 525/60 standard.

In accordance with the present invention
15 (Claim 1), a component signal of 625/50 television
standards is converted into a component signal of 525/60
television standards in the above described configura-
tion as described below. That is to say, the field
frequency is converted from 50 Hz to 60 Hz in the time-
20 axis compression and field frequency conversion means
without decimating scanning lines by compressing a
signal on the time axis. Thereafter, scanning line
interpolation processing for converting odd/even field
attribute and converting spatial positions of scanning
25 lines is performed by the scanning line interpolation
means. Further, in the time-axis expansion and scanning
line number conversion means, the number of scanning
lines is converted from 625 to 525 by decimating

1 unnecessary scanning lines included in the scanning
lines interpolated by the scanning line interpolation
means and the signal is expanded on the time axis to
restore the rate of the original clock and output the
5 resultant signal. As a result, television standards
conversion causing less picture quality degradation
becomes possible.

In accordance with the present invention
(Claim 2), a component signal of 625/50 television
10 standards is converted into a component signal of 525/60
television standards as described below. By the field
frequency and scanning line number conversion means, the
number of scanning lines and the field frequency are
respectively converted from 625 and 50 Hz to 525 and 60
15 Hz by means of scanning line decimation processing and
repetition of the signal with a field taken as the unit,
and the resultant signal is derived from the first out-
put of the digital memory. In the scanning line inter-
polation means, scanning line interpolation processing
20 for converting odd/even field attribute and converting
spatial positions of scanning lines is performed by
deriving, from the second output of the digital memory,
a signal which is 1H away from the signal derived from
the first output. As a result, television standards
25 conversion causing less picture quality degradation
becomes possible.

1 BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 is a block diagram showing the configuration of a scanning line number and field frequency conversion circuit of an embodiment (Claim 1) 5 of a television standards conversion apparatus according to the present invention;

Fig. 2 is a block diagram of a scanning line interpolation circuit in an embodiment (Claim 1) of the present invention;

10 Fig. 3 is a diagram for explaining control of a field memory in an embodiment of the present invention;

Fig. 4 is a diagram for explaining control of a line memory in an embodiment (Claim 1) of the present 15 invention;

Figs. 5A-5D are schematic diagrams showing an example of scanning line interpolation processing for converting odd/even field attribute and converting spatial positions of scanning lines in an embodiment of 20 the present invention;

Fig. 5A is a schematic diagram showing processing of interpolating scanning lines of odd fields of the 525/60 standard on the basis of scanning lines of odd fields of the 625/50 standard;

25 Fig. 5B is a schematic diagram showing processing of interpolating scanning lines of even fields of the 525/60 standard on the basis of scanning lines of even fields of the 625/50 standard;

1 Fig. 5C is a schematic diagram showing
processing of interpolating scanning lines of even
fields of the 525/60 standard on the basis of scanning
lines of odd fields of the 625/50 standard;

5 Fig. 5D is a schematic diagram showing
processing of interpolating scanning lines of odd fields
of the 525/60 standard on the basis of scanning lines of
even fields of the 625/50 standard;

10 Fig. 6 is a block diagram showing the
configuration of a scanning line number and field
frequency conversion circuit of another embodiment
(Claim 2) of a television standards conversion apparatus
according to the present invention;

15 Fig. 7 is a block diagram of a scanning line
interpolation circuit in another embodiment (Claim 2) of
the present invention;

Fig. 8 is a diagram for explaining control of
a field memory in another embodiment of the present
invention;

20 Fig. 9 is a schematic diagram showing an
example of conventional scanning line interpolation
processing; and

25 Fig. 10 is a diagram for explaining how
conventional field frequency conversion is performed by
repetition of a field unit.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment (Claim 1) of the present

1 invention will hereafter be described by referring to
the drawing.

Fig. 1 is a block diagram showing the configuration of a scanning line number and field frequency conversion circuit included in an embodiment of a television standards conversion apparatus according to the present invention. In Fig. 1, numeral 1 denotes an input terminal. Digitized component signals of a television standards (625/50 standard) to be converted are multiplexed and inputted to the input terminal 1. Numeral 2 denotes a field memory. By writing signals into the field memory 2 with a clock of a clock generator 6 and reading signals from the field memory 2 with a clock of a clock generator 7 generating the clock having a frequency which is 6/5 times the clock frequency of the clock generated by the clock generator 6, signal compression on the time axis is performed. Together therewith, repetitive readout of the signal of the field unit is performed according to a control signal supplied from a memory control circuit 5, the field frequency being thus converted. Numeral 3 denotes a scanning line interpolation circuit. The scanning line interpolation circuit 3 operates with the clock of the clock generation circuit 7, and performs scanning line interpolation processing for converting odd/even field attribute and converting spatial positions of scanning lines on the output signal of the field memory 2. Numeral 4 denotes a line memory. Signals are

1 written into the line memory 4 with the clock of the
clock generator 7, and signals are read from the line
memory 4 with the clock of the clock generator 6.

Scanning line decimation and signal expansion on the
5 time axis are thus performed on the output signal of the
scanning line interpolation circuit 3 according to a
control signal supplied from a memory control circuit 8.
A component signal converted to the 525/60 standard is
outputted to an output terminal 9.

10 Assuming that the television signals so
inputted to the input terminal 1 as to be converted are
multiplexed PAL component signals of the 625/50 standard
and those signals are converted to multiplexed NTSC
component signals of 525/60 standard and outputted to
15 the output terminal 9, operation of the above described
configuration will now be described.

When digitized and multiplexed component
signals of the PAL standard are inputted at the input
terminal 1, the input PAL signals are written into the
20 field memory 2 by the clock of the clock generator 6.
Writing signals into the field memory 2 and reading
signals from the field memory 2 are conducted for the
memory address corresponding to control signals for
controlling the write address and the read address
25 outputted from the memory control circuit 5. The
relation between the write address and the read address
of the field memory 2 controlled by the memory control
circuit 5 is shown in Fig. 3. As for the signal stored

1 in the field memory 2 having the write address and read
address controlled as shown in Fig. 3, the signal of one
field unit is read out repetitively every five fields.
That is to say, the signal corresponding to six fields
5 is outputted in the interval of five fields of the input
PAL signal. Thereby the field frequency is converted
from 50 Hz to 60 Hz. If reading is conducted at the
time of reading by the same clock as that of writing,
the quantity of the signal read out in one frame
10 interval is limited to five-sixths because the field
frequency has been increased to six-fifths. That is to
say, only five-sixths of 625 scanning lines of the PAL
signal per frame can be read out. Therefore, a clock
generator 7 for generating a clock having a frequency
15 equivalent to six-fifths of the clock frequency of the
clock generator 6 is used. By reading a signal from the
field memory 2 with the clock of the clock generator 7
having a rate equivalent to six-fifths of that of the
clock used to write the signal into the field memory 2,
20 the signal is compressed to five-sixths on the time
axis. Even if the signal of field unit is repetitively
read out at the rate of one field every five fields, all
of 625 scanning lines of the PAL signal per frame can
thus be read out. By doing so, the signal can be read
25 out from the field memory 2 without decimation even if
the field frequency is converted from 50 Hz to 60 Hz.
Therefore, picture quality degradation of converted
images due to signal decimation can be prevented.

1 The signal subjected to time-axis compression
and field frequency conversion has been subjected to
repetitive signal processing of field unit for field
frequency conversion when that signal is read out from
5 the field memory 2. In the same way as the example
shown in Fig. 10, therefore, odd fields and even fields
are not arranged alternately and correctly.

In the scanning line interpolation circuit 3,
therefore, scanning line interpolation processing is so
10 conducted that odd fields and even fields may be
alternately outputted correctly. The configuration of
the scanning line interpolation circuit 3 is shown in
Fig. 2. When the signal read out from the field memory
2 is inputted to an input terminal 31 of the scanning
15 line interpolation circuit 3, the input signal is so
weighted by a coefficient multiplier 32 as to be
increased k times. Further, a signal delayed in a 1H
delay unit 33 by 1H as compared with the input signal is
so weighted by a coefficient multiplier 34 as to be
20 increased $(1-k)$ times. The input signal increased k
times and the 1H delay signal increased $(1-k)$ times are
added together by an adder 36, and the resultant sum
signal is outputted from an output terminal 37 as an
interpolation signal. The weighting coefficient k for
25 scanning line interpolation depends upon the relative
positions of inputted scanning lines and interpolated
scanning lines, and it can be selected out of five
values: 1, $3/4$, $2/4$, $1/4$ and 0. Weighting coefficients

1 corresponding to scanning line positions are stored in a
weighting coefficient ROM 35. Scanning line interpolation
processing is processing for correcting the difference
in spatial position between the PAL signal and the
5 NTSC signal. In the present example, however, conversion
of odd/even field attribute is also conducted at
the same time. That is to say, scanning line interpolation
processing is so performed that fields of the
output signal may keep the field sequence relation as
10 described below. When odd fields and even fields of the
signal read out from the field memory 2 are arranged
correctly in order, odd field scanning lines of the
525/60 standard are interpolated on the basis of odd
field scanning lines of the 625/50 standard as shown in
15 Fig. 5A or even field scanning lines of the 525/60
standard are interpolated on the basis of even field
scanning lines of the 625/50 standard as shown in Fig.
5B. When odd fields and even fields of the signal read
out from the field memory 2 have interchanged order,
20 even field scanning lines of the 525/60 standard are
interpolated on the basis of odd field scanning lines of
the 625/50 standard as shown in Fig. 5C or odd field
scanning lines of the 525/60 standard are interpolated
on the basis of even field scanning lines of the 625/50
25 standard as shown in Fig. 5D. Scanning line interpolation
processing according to conversion of the odd/even
field attribute is thus performed. By thus switching
four ways of scanning line interpolation processing, odd

1 fields and even fields are outputted alternately and
correctly. Switching of scanning line interpolation
processing is implemented by preparing weighting
coefficients k corresponding to four ways of scanning
5 line interpolation processing in the weighting
coefficient ROM 35 of the scanning line interpolation
circuit 3 and making a selection out of those weighting
coefficients according to the scanning line interpola-
tion processing. In the same way as the example of Fig.
10 9, not only 525 scanning lines needed as the NTSC signal
are interpolated but also a signal which is not neces-
sary as the NTSC is interpolated at the rate of one
scanning line approximately every six scanning lines, on
the basis of 625 scanning lines per frame inputted to
15 the scanning line interpolation circuit 3. Therefore,
625 scanning lines in total per frame are outputted from
the scanning line interpolation circuit 3.

The signal outputted from the scanning line
interpolation circuit 3 is inputted to the line memory
20 4. Writing a signal into the line memory 4 is conducted
by the clock of the clock generator 7. At the time of
outputting, reading the signal from the line memory 4 is
conducted by the clock of the clock generator 6. As
described before, the clock of the clock generator 6 has
25 a frequency equivalent to five-sixths of that of the
clock of the clock generator 7. Therefore, the signal
outputted from the line memory 4 is expanded on the time
axis and the clock rate is restored to the rate used at

1 the time of input. At this time, the write address and
read address of the line memory 4 are controlled by the
memory control circuit 8 as shown in Fig. 4. Whereas
625 scanning lines per frame are written into the line
5 memory 4, scanning lines are read out while they are
being decimated at the rate of one scanning line every
six scanning lines. As a result, 525 scanning lines per
frame are outputted. The memory control circuit 8
controls the write address and read address of the line
10 memory 4 so that scanning lines decimated at this time
may become 100 scanning lines per frame which are
included in 625 scanning lines per frame interpolated by
the scanning line interpolation circuit 3 and which are
not needed as the NTSC signal. In this way, multiplexed
15 component signals converted into the NTSC standard with
the field frequency of 60 Hz and the number of scanning
lines of 525 are outputted to an output terminal 9.

In the present embodiment heretofore
described, the signal is temporarily compressed on the
20 time axis in the course of processing by using different
clocks for digital memory writing and reading operation.
Thereby, conversion of the field frequency can be
realized without losing a signal. As a result, degrada-
tion of the converted picture quality can be suppressed.
25 Further, by switching scanning line interpolation
processing so that the field sequence relation of the
converted output signal may always hold good, converted
images with less flicker are obtained.

1 Subsequently, another embodiment (Claim 2) of
the present invention will be described by referring to
the drawing.

Fig. 6 is a block diagram showing the configuration of a scanning line number and field frequency conversion circuit included in another embodiment of a television standards conversion apparatus according to the present invention. In Fig. 6, numeral 1 denotes an input terminal. Digitized and multiplexed component signals of the 625/50 standard are inputted to the input terminal 1. Numeral 10 denotes a field memory. Signals are written into or read from the field memory 10 by the clock of the clock generator 6. The signal of a field unit is repetitively read out according to a control signal fed from a memory control circuit 12, the field frequency being converted. The field memory 10 is a memory having two independent output standards. Via respective outputs, signals can be read out from different memory addresses. Numeral 11 denotes a scanning line interpolation circuit. With respect to the output signal of the field memory 10, the scanning line interpolation circuit 11 conducts the scanning line interpolation processing for converting the odd/even field attribute and converting the spatial positions of scanning lines. Further, the scanning line interpolation circuit 11 outputs multiplexed component signals converted to the 525/60 standard to the output terminal 9.

Assuming that the television signals so

1 inputted to the input terminal 1 as to be converted are
multiplexed PAL component signals of the 625/50 standard
and those signals are converted to multiplexed NTSC
component signals of 525/60 standard and outputted to
5 the output terminal 9, operation of the above described
configuration will now be described. When digitized and
multiplexed component signals of the PAL standard are
inputted at the input terminal 1, the input PAL com-
ponent signals are written into the field memory 10 by
10 the clock of the clock generator 6. Writing signals
into the field memory 10 and reading signals from the
field memory 10 are conducted for the memory address
corresponding to control signals for controlling the
write address and the read address outputted from the
15 memory control circuit 12. The relation between the
write address and the read address of the field memory
10 controlled by the memory control circuit 12 is shown
in Fig. 8. As for the signal stored in the field memory
10 having the write address and read address controlled
20 as shown in Fig. 8, the signal of one field unit is read
out repetitively every five fields. That is to say, the
signal corresponding to six fields is outputted in the
interval of five fields of the input PAL signal. There-
by the field frequency is converted from 50 Hz to 60 Hz.
25 By increasing the field frequency 6/5 times, the
quantity of the signal read out from one output of the
field memory 10 in one frame interval is limited to
five-sixths. That is to say, only five-sixths of

1 inputted 625 scanning lines of the PAL signal per frame
can be read out. In reading a signal from the field
memory 10, therefore, scanning lines are decimated at
the rate of one scanning line approximately every six
5 scanning lines. From one output, 525 scanning lines per
frame are outputted with the field frequency of 60 Hz.
The output signal of the field memory 10 undergoes
scanning line interpolation processing in the scanning
line interpolation circuit 11. The configuration of the
10 scanning line interpolation circuit 11 is shown in Fig.
7. Since the scanning line interpolation processing is
processing for interpolating an NTSC scanning line on
the basis of two PAL scanning lines which are 1H away
from each other, read addresses of the two output
15 standards are so controlled by the memory control
circuit 12 that signals which are 1H away from each
other may always be read out from two outputs of the
field memory 10. In addition, read addresses are so
controlled that PAL scanning lines corresponding to the
20 NTSC scanning line interpolated by the scanning line
interpolation processing, i.e., PAL scanning lines
spatially adjacent to the interpolated NTSC scanning
line may be outputted from respective outputs. The
signal fed from the second output of the field memory 10
25 is always delayed by 1H as compared with the signal fed
from the first output. Therefore, the signal fed from
the first output of the field memory 10 is the signal of
the lower scanning line spatially adjacent to the

1 interpolated NTSC scanning line, whereas the signal fed
from the second output of the field memory 10 is the
signal of the upper scanning line spatially adjacent to
the interpolated NTSC scanning line.

5 The signal read out in the above described
relation and fed from the first output of the field
memory 10 is inputted to an input terminal 38 of the
scanning line interpolation circuit 11. The signal fed
from the second output of the field memory 10 is
10 inputted to an input terminal 39 of the scanning line
interpolation circuit 11. The signals fed to the input
terminals 38 and 39 are increased in magnitude k times
and $(1-k)$ times by coefficient multipliers 32 and 34,
respectively. The resultant signals are added together
15 in an adder 36 and outputted to an output terminal 37.
The weighting coefficient k for scanning line inter-
polation depends upon the relative positions of inputted
scanning lines and interpolated scanning lines, and it
can be selected out of five values: 1, $3/4$, $2/4$, $1/4$ and
20 0. Weighting coefficients corresponding to scanning
line positions are stored in a weighting coefficient ROM
35. Scanning line interpolation processing is proces-
sing for correcting the difference in spatial position
between the PAL signal and the NTSC signal. However,
25 conversion of odd/even field attribute is also conducted
at the same time. The signal read out from the field
memory 10 has been subjected to repetitive readout of
signal of a field unit at the rate of one field every

1 five fields for field frequency conversion. In the same
way as the example shown in Fig. 10, therefore, odd
fields and even fields are not arranged alternately and
correctly. In the scanning line interpolation circuit
5 11, therefore, scanning line interpolation processing is
so switched that fields of the output signal may keep
the field sequence relation. That is to say, scanning
line interpolation processing is performed as described
below. When odd fields and even fields of the output
10 signal of the field memory 10 are arranged correctly in
order, odd field scanning lines of the 525/60 standard
are interpolated on the basis of odd field scanning
lines of the 625/50 standard as shown in Fig. 5A or even
field scanning lines of the 525/60 standard are inter-
15 polated on the basis of even field scanning lines of the
625/50 standard as shown in Fig. 5B. When odd fields
and even fields of the output signal of the field memory
10 have interchanged order, even field scanning lines of
the 525/60 standard are interpolated on the basis of odd
20 field scanning lines of the 625/50 standard as shown in
Fig. 5C or odd field scanning lines of the 525/60
standard are interpolated on the basis of even field
scanning lines of the 625/50 standard as shown in Fig.
25 5D. Scanning line interpolation processing according to
conversion of the odd/even field attribute is thus
performed, 525 NTSC scanning lines being thus inter-
polated. By thus switching four ways of scanning line
interpolation processing, odd fields and even fields are

1 outputted alternately and correctly. Switching of
scanning line interpolation processing is implemented by
preparing weighting coefficients k corresponding to four
ways of scanning line interpolation processing in the
5 weighting coefficient ROM 35 of the scanning line
interpolation circuit 11 and making a selection out of
those weighting coefficients according to the scanning
line interpolation processing. In this way, multiplexed
component signals converted to the NTSC standard with
10 the field frequency of 60 Hz and the number of scanning
lines of 525 are outputted to the output terminal 9.

In the present embodiment heretofore
described, it is possible to read out efficiently the
signal required to interpolate scanning lines and
15 achieve conversion of the field frequency by using the
digital memory having two output standards. Therefore,
degradation of the converted picture quality can be
suppressed. Further, by switching scanning line inter-
polation processing so that the field sequence relation
20 of the converted output signal may always hold good,
converted images with less flicker are obtained.

As evident from the embodiments heretofore
described, the present invention makes it possible to
provide a television standards conversion apparatus free
25 from flickers due to inversion of odd fields and even
fields and free from picture quality degradation due to
lowering in precision of scanning line interpolation
resulting from decimation of scanning lines.

1 The present invention is not limited to the
aspects of the above described embodiments.

CLAIMS

1. A television standards conversion apparatus comprising:

clock generation means for generating a first clock and a second clock;

time-axis compression and field frequency conversion means for performing time-axis compression on a signal and converting a field frequency of the 625/50 television standards to a field frequency of the 525/60 television standards by writing a digitized component signal of 625/50 television standards into a first digital memory with the first clock generated by said clock generation means and reading the signal from said first digital memory with the second clock generated by said clock generation means;

scanning line interpolation means for performing scanning line interpolation processing for converting odd/even field attribute and converting spatial positions of scanning lines on said signal compressed on the time axis and converted in field frequency; and

time-axis expansion and scanning line number conversion means for expanding the signal on the time axis by writing said signal having interpolated scanning lines into a second digital memory with the second clock generated by said clock generation means and reading the signal from said second digital memory with the first clock generated by said clock generation means, and for

converting the number of scanning lines to that of the 525/60 standard by means of scanning line decimation processing.

2. A television standards conversion apparatus comprising:

field frequency and scanning line number conversion means for writing a digitized component signal of 625/50 television standards into a digital memory having two output standards allowing readout from mutually independent addresses, for converting the field frequency and the number of scanning lines to the field frequency and the number of scanning lines of the 525/60 television standards when reading the signal from said digital memory, and for deriving the resultant signal from a first output terminal;

memory control means for deriving, from a second output of said digital memory, a signal which is 1H away from said signal subjected to the conversion in field frequency and the number of scanning lines and derived from the first output of said digital memory; and

scanning line interpolation means for performing scanning line interpolation processing for converting odd/even field attribute and converting spatial positions of scanning lines on said signal converted in field frequency and derived from said first output, by using said signal which is 1H away derived from said second output, and for thereby converting said

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signal converted in field frequency into a signal of
525/60 standard.

Patents Act 1977
Examiner's report to the Comptroller under
Section 17 (The Search Report)

29.

Application number

9206070.6

Relevant Technical fields

(i) UK CI (Edition K) H4F (FEP)

(ii) Int CI (Edition 5) H04N

Search Examiner

J COULES

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search

24 JULY 1992

Documents considered relevant following a search in respect of claims

1

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	EP 0323198 A2 (NEC) - see frame and line number converters 30, 35, Figure 3	1
A	GB 1391434 (BBC) - whole document and see reference to GB 1052438 on page 3 lines 52-57	1
A	GB 1052438 (BBC)	1

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

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